

Amendments to the Specification:

Please amend the paragraph beginning at page 7, line 9, as follows:

In certain embodiments of the invention different gate dielectric layers are formed on a wafer comprising shallow trench isolation regions. FIG. 8 illustrates a wafer 50 150 comprising a silicon base layer 42 152 and a plurality of shallow trench isolation regions 54 154. A gate oxide layer 56 156 is formed on the silicon base layer 42 152 by thermal oxidation of silicon layer 42 152 or by silicon oxide deposition techniques. After the formation of the gate oxide layer 56 156, a mask is formed over the wafer 50 150 and selected first portions of the gate oxide layer 56 156 are removed by etching. A first alternate dielectric is subsequently deposited where the first portions of the gate oxide layer 56 156 were removed. Alternate dielectrics include high-k dielectrics, nitride stack dielectrics, and other known dielectrics. After depositing the first alternate dielectric, the wafer 50 150 is again masked and second portions of the gate oxide layer 56 156 are removed by etching. A second alternate dielectric is deposited where the second portions of the gate oxide layer were removed. Masking, etching, and alternate dielectric deposition is repeated until a desired number of different types of dielectric layers are deposited. An exemplary embodiment comprising different types of gate dielectrics is shown in FIG. 9, which comprises a high-k dielectric layer 60 160, a nitride stack dielectric layer 58 158, and a gate oxide layer 56 156.

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